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Applicant: Leonard Forbes et al.

Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Docket No.: 303.586US1
Filed: May 26, 1999
Examiner: Anh-Quan Tra

Serial No.: 09/320,421
Due Date: ~~June 22~~, 2001
Group Art Unit: 2816

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We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response under 37 CFR 1.116 (14 Pages).
X Copy of 1 supporting reference (US Patent No. 6,104,068) (9 pgs.).
X Clean Version of Pending Claims (11 pgs.).

If an additional fee is required due to changes to the claims, the fee has been calculated as follows:

| CLAIMS AS AMENDED | | | | | | |
|---|---|---|---|---|---|---|
| | (1) Claims Remaining After Amendment | | (2) Highest Number Previously Paid For | (3) Present Extra | Rate | Fee |
| TOTAL CLAIMS | 39 | - | 45 | | x 18 = | $0.00 |
| INDEPENDENT CLAIMS | 12 | - | 12 | | x 80 = | $0.00 |
| [ ] MULTIPLE DEPENDENT CLAIMS PRESENTED | | | | | | $0.00 |
| TOTAL | | | | | | $0.00 |

**Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.**

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By:
Atty: Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner for Patents, Washington, D.C. 20231, on this 12th day of April, 2001.

Amy Moriarty
Name

Amy Moriarty
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**Customer Number 21186**
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)
(GENERAL)

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**EXPEDITED PROCEDURE - EXAMINING GROUP 2816**

S/N 09/320,421 **PATENT**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|---|
| Applicant: | Leonard Forbes et al. | Examiner: | Anh-Quan Tra |
| Serial No.: | 09/320,421 | Group Art Unit: | 2816 |
| Filed: | May 26, 1999 | Docket: | 303.586US1 |
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**AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116**

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In response to the final Office Action mailed March 22, 2001, please amend the application as follows:

**IN THE DRAWINGS**

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dual-gated transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

As addressed in the previous office action, Figures 2A and 3 of the Applicant's drawing set illustrate a pair of "dual-gated" transistors. One dual-gated transistor is represented by the combination of M3 and M5 having a shared body region, a single source region 208, and single drain region 204, and two gates 223 and 254 respectively on opposing sides of the shared body region. The other dual gated transistor, as defined on page 10, line 16-20 of the Applicant's specification, is comprised of the combination of M4 and M6 having a shared body region, a single source region 210, and single drain region 206, and two gates 225 and 253 respectively on opposing sides of the shared body region. It has been explained that the dual-gated transistors in the Applicant's case involve two gates on opposing sides of the body region such that the combination is in fact "dual-gated," and in such a configuration do perform the OR function in contrast to the Cuevas reference. The Examiner continues to point to the dual gate configuration shown in Cuevas which illustrates two gates on the same side of the transistor body performing the AND function. Applicant has clearly provided a reference for the Examiner, by the same inventor in US patent number 6,104,068 which further supports the Applicant's lexicography. A